

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 09/11/09 was filed after the mailing date of the Non-Final Office Action on 05/29/09. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slater US 4,872,106 (provided by Applicant) in view of Vekiarides, N. "Fault-Tolerant Disk Storage and File Systems Using Reflective Memory". Proceedings of the 28th Annual Hawaii International Conference on System Sciences (1995): 103-113.

Slater discloses:

18. A method for operating a redundant automation system for controlling a technical device (e.g., col. 1 lines 11-16), comprising:

operating a first automation device as a master (e.g., Fig. 2, col. 3 line 35: “primary processor”);

operating a second automation device as a standby (e.g., Fig. 2, col. 4 line 58: “back-up processor”);

storing status data of the first and second automation devices in a ~~reflective~~ memory unit (e.g., Fig. 2 #46, col. 5 line 60 – col. 6 line 14) wherein a common memory area of the ~~reflective~~ memory unit can be written to and read from both said first and said second automation devices, wherein the data present in the common memory area is available in parallel and in real time to the automation devices (e.g., col. 2 lines 1-4, col. 6 lines 39-64);

sensing, with the use of a monitoring module operatively coupled to both said first and said second automation devices (e.g., col. 5 lines 46-59), for the presence of a vital sign from said first automation device for a change and when no change is sensed during a given cycle of operation, then making a switchover to the standby automation device that takes over the function of the former master automation device (e.g., col. 7 line 45 – col. 8 line 7); and,

wherein there is present in the common memory area of the ~~reflective~~ memory unit status data which describes the current operating status of the technical device and the automation system immediately before a technical device error occurs in the master automation device (e.g., col. 5 line 60 - col. 6 line 14, col. 6 lines 39-64).

16. The method as claimed in claim 18, wherein the switchover is performed in a jolt-free manner such that a portion of the data residing in the common memory area of the ~~reflective~~

memory unit is immediately processed by the standby automation device as the current status image of the technical device and the automation system (e.g., col. 6 line 39 - col. 7 line 7).

As noted above via strikethrough, Slater does not explicitly disclose that the memory unit is a reflective memory unit.

Vekiarides discloses dual controllers connected via a reflective memory (e.g., Fig. 3, Fig. 4, Section 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Slater with Vekiarides since the substitution of one known element (a generic dual port memory with a specific reflective memory) for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention. See *KSR v. Teleflex*, 127 S.Ct. 1727 (2007).

One would have been motivated to make such a modification, i.e., substitute the dual port memory of Slater with the reflective memory of Vekiarides, since Vekiarides teaches that reflective memory interconnected computers are well suited to building large scale fault-tolerant disk storage and file systems for I/O intensive applications. The modularity of both computational nodes and input/output controller nodes allows nodes to be removed or added to a Reflective Memory configuration without any down time in the remaining nodes. This modularity in a massively parallel architecture yields a very robust disk storage and file system. The broadcast capabilities of the Reflective Memory allow redundant operations, critical to achieving fault tolerance, to occur at speeds approaching conventional systems (Section 5).

One would have also been motivated to make such a modification since Vekiarides teaches that a reflective memory allows for the dual controllers and disk subsystems to be located in separated rooms or even separate buildings using a fiber-optic link between the controllers (pg. 109 col. 1).

Response to Arguments

Applicant's arguments filed 08/24/09 have been fully considered but they are not persuasive. Examiner disagrees with Applicant's argument on two counts. First, Examiner disagrees with Applicant's characterization of the "System Sciences Proceedings" reference (hereinafter referred to as "Vekiarides"). Second, even assuming, *in arguendo*, that Applicant's characterization of the Vekiarides references is accurate, Examiner asserts that it would still not preclude a proper holding of obviousness.

On the first count, Examiner disagrees with Applicant's characterization of the Vekiarides reference. Applicant is equating Vekiarides's design objective of "no standby modules" with no utilization of back-up modules (pg. 3 line 22 of Arguments). However, the term "standby" has two general meanings in the art. It can mean "idle" or it can mean "back-up". Examiner asserts that Vekiarides is using the term here to mean "no idle modules". This assertion is further corroborated by other sections of the reference, which clearly disclose the use of back-up or redundant or mirrored systems. For example, see page 108 col. 2, where Vekiarides discloses a "backup controller", or "fully replicated dual controller".

On the second count, even assuming, *in arguendo*, that Applicant's characterization of the Vekiarides references is accurate, it is noted that the test for obviousness is not whether the

features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case, Examiner is not trying to bodily incorporate the entire structure of the secondary Vekiarides reference into the structure of the primary reference Slater. The primary reference Slater is complete unto itself, with the exception that it is merely missing a teaching of reflective memory. Vekiarides has been provided only to teach that feature which is missing from Slater, nothing more and nothing less. Vekiarides also provides motivation for why someone would want to employ reflective memory in their system. Lastly, the modification of Slater has done nothing to render it unsatisfactory for its intended purpose, as suggested by Applicant.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN A. JARRETT whose telephone number is (571)272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan A. Jarrett/
Primary Examiner, Art Unit 2121

10/29/09